REMARKS

Claims 1-21 and 24 are pending, with claims 1 and 12 being independent. Claims 22 and 23 have been cancelled. Reconsideration and allowance of the above-referenced application are respectfully requested.

Rejections Under 35 U.S.C. §103

Claims 1 to 8 and 11 to 21 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. 5,983,350 issued to Minear (hereinafter "Minear"), and further in view of U.S. Patent No. 6,959,346 issued to Low (hereinafter "Low).

Claims 9 and 24 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Minear and Low, and further in view of U.S. Patent Publication No. 2004/0160903 by Applicant Gai (hereinafter "Gai").

Claim 10 stands rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Minear and Low, and further in view of U.S. Patent No. 6,426,706 issued to King (hereinafter "King").

These rejections and their underlying rationale are traversed. Applicant's claims are allowable over any hypothetical combination of these references. As noted in the previous response mailed December 3, 2007, the proposed Minear-Low combination does not teach or suggest each and every element of claim 1. For example, the proposed Minear-Low combination does not teach or suggest "a first high-speed crypto system which operates using dedicated hardware components for cryptographic encryption and decryption of a first format kind of message, a second high-speed crypto system physically separate from said first high-speed crypto system using dedicated hardware components for cryptographic encryption and decryption of a second format kind of message different than said first format kind of message" as recited in claim 1.

In that regard, the Examiner's statement in the "Response to Arguments" section of the Office Action is respectfully traversed.[1] For example, the Examiner states that "[i]t is also specifically mentioned in Low that cipher processing involves encryption and decryption (see for example col. 6 lines 36 to 51 and col. 7 line 26 to 35)."[2] Contrary to the Examiner's assertion, col. 6 lines 36 to 51 of Low describes a "cipher processor [that] **decrypts** the packet data" and col. 7 line 26 to 35 of Low does not talk about cipher processor, but describes a "**DES encryption engine** [that] strip[s] the header from a packet and provide[s] the data to be encrypted by the processor ...." Because Low's cipher processor and the DES encryption engine are different components, Low does not disclose a cipher processor that performs **both** encryption and decryption functions as required by claim 1.

Further, Low specifically states that the cipher processor is used for decryption only; nowhere does Low disclose using the cipher processor for encryption. *See, e.g.*, Col. 5, lines 44-50 of Low, which states that "Referring to FIG. 2, a simplified flow diagram of a method of packet processing for a packet received at input port 12 is shown. The packet is received. It is classified to determine a packet format. Here, the format is encrypted so the **encrypted packet data is provided to a cipher processor for decryption**." (Emphasis added.) In addition, the DES encryption engine of Low is used only for encryption; there is simply no teaching or suggestion that the DES encryption engine is used for decryption.

In addition, each of Low's processors cannot be equated to the crypto system of claim 1 because, e.g., claim 1 requires the crypto system to include "dedicated hardware components." Low's processor, in contrast, does not include such hardware components. As noted previously, Low discloses multiple processors with each processor dedicated to perform a specific function, e.g., classification, cipher processing, and combining packets; and Examiner appears to equate each processor of Low as the crypto system of claim 1. However, because each processor in Low performs a specific function and does not include "dedicated hardware components," each of Low's processors is not the same as the crypto system as claimed.

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[1] Office Action dated 3/3/2008 at page 2.
[2] *Id.* at pages 2-3.

Even if arguendo each of Low's processors could be equated to the crypto system as claimed, which the Applicant does not concede, the individual processors disclosed by Low does not perform both encryption and decryption. As noted above, Low does not teach or suggest a processor that performs **both cryptographic encryption and decryption**.[3] In fact, nowhere does Low teach or suggest having **two crypto systems** with each dedicated to operate cryptographic encryption and decryption on a different format kind of message. This is because having two crypto systems for performing **both cryptographic encryption and decryption** would be contrary to the object of Low, which is to "provide a flexible processor architecture for supporting encryption and other processing of data within a data stream."[4] Low simply does not contemplate using two processors to perform the same function, i.e., cryptographic encryption and decryption.

One potential application of the system of claim 1 is to provide a number of different optimized and unoptimized encryption and decryption structures that can be used for different items. Claim 1, defines first and second high speed crypto systems. These two crypto systems are used for different formats of messages. Since one crypto system is used for one format and another for another format, these formats of crypto systems can be handled very quickly in this hardware. As noted above, Low does not disclose this claimed subject matter of first and second high speed crypto systems, which use **dedicated hardware components for cryptographic encryption and decryption** of a special format. Thus, the proposed Minear-Low combination

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[3] *See, e.g.*, Claim 8 of Low, which states "wherein **respective processors** perform IP header manipulation and encryption;" see also, Claim 10 of Low, which states "A method of **encrypting or decrypting data packets** comprising: modifying a received packet to include control data which includes **a list of processes to be performed on the packet**; forwarding the packet from processor to processor through an interconnection including a buffer controller which responds to control data in the packets to determine a **processor of the plurality of processors dedicated for processing a process** in the list of processes; and in successive processors, performing the processes identified by the control data, including **an encryption or decryption process**."

[4] Col. 3, lines 54-56; see also, e.g., Col. 7, lines 19-25, which states that "Typically client processors 54 are **dedicated to a single form of processing** that is self contained and can be performed on a packet in isolation. **Cipher processing is one such process**. Thus, a **DES encryption engine** typically **forms a client processor** for receiving data, for encrypting the data, and for returning the encrypted data to the SPB." (emphases added); see also, e.g., FIG. 8 and Col. 8, lines 29-36, which states that "The next process is that process indicated by control 3, **3DES Encryption**. Client 84 provides this functionality. The super packet is provided to **client 84** where, as shown in FIG. 9b **encryption is performed and the function control 3 is marked as having been performed.**" (emphases added).

does not teach or suggest "a first high-speed crypto system which operates using dedicated hardware components for cryptographic encryption and decryption of a first format kind of message, a second high-speed crypto system physically separate from said first high-speed crypto system using dedicated hardware components for cryptographic encryption and decryption of a second format kind of message different than said first format kind of message" as recited in claim 1.

Therefore, claim 1 is patentably distinct from Minear and Low, either alone or in combination, and claim 1 is allowable for at least the reasons discussed above.

In addition, independent claim 12 also recites "a high-speed crypto system formed of hardware encryption parts including a first high-speed crypto part using dedicated hardware components for cryptographic encryption and decryption of a first format kind of message, a second high-speed crypto part physically separate from said first high-speed crypto part, using dedicated hardware components for cryptographic encryption and decryption of a second format kind of message, different than said first format kind of message" and is thus patentably distinguishable over the proposed Minear-Low combination for analogous reasons to those discussed for independent claim 1. Furthermore, because claims 2-11, 13-21, and 24 depend generally from claim 1 or 12, these dependent claims are patentably distinguishable over the proposed Minear-Low combination for at least the reasons provided above.

Thus, all the pending claims are allowable for at least the reasons provided above.

Concluding Comments

It is believed that all of the pending claims have been addressed in this paper. However, failure to address a specific rejection, issue or comment, does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above are not intended to be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated

in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Applicants ask that all claims be allowed. Please apply applicable charges or credits to Deposit Account No. 06-1050.

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